

REMARKS

Applicants have amended claims 1-5 solely to improve English usage without changing claim scope. The recitation of “an amplifier” in claim 4 merely recites a limitation inherent in “an amplifier circuit,” and the recitation of “an optical element” in claim 5 merely recites a limitation inherent in “an optical pickup.” The detailed circuit connections of the claimed amplifier and optical element are shown in FIGS. 4 and 6 of the application. Finally, since the claims are open, there is no difference in coverage between reciting “a” device or transistor and “one or more” devices or transistors.

Applicants thank the Examiner for indicating the presence of allowable subject matter.

Claim 1 has been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 5,854,772 (Suzu). Applicants respectfully traverse this rejection.

Original claim 1 stated that the collector of the P-type transistor is an output terminal of the first control output and the collector of the N-type transistor is an output terminal of the second control output. Accordingly, original claim 1 requires two output terminals for the first and second control outputs. The preamble of claim 1 also explains that the claimed decoder circuit decodes an input voltage into three or more control outputs. Simply in the interest of clarity, applicants have amended claim 1 to state that the P-type transistor comprises a collector (drain) configured to be a first output terminal of the first control output and the N-type transistor comprises a collector (drain) configured to be a second output terminal of a second control output. Because the claimed decoder has two output terminals, they can provide two different control outputs at the same time. See, for example, page 18, lines 8-20, and FIG. 4 of the application.

The Examiner contends that Suzu’s NANDA1 corresponds to the claimed decoder circuit. Specifically, the Examiner seems to contend that Suzu’s p-channel transistors QA01-QA03 correspond to the claimed P-type transistor and Suzu’s n-channel transistors QA04-QA06 correspond to the claimed N-type transistor. See paragraph 2 of the Action. However, Suzu’s p-

channel and n-channel transistor are configured to operate collectively to produce one output signal at a time. See column 2, lines 7-41, of Suzu. Accordingly, Suzu's transistors QA01-06, which the Examiner equates to the claimed P-type and N-type transistors, have only one output terminal, the "output signal wire" that supplies Suzu's output signal to Suzu's INVA1. See, for example, column 1, lines 26-45, and FIG. 1 of Suzu. On the contrary, the claimed decoder circuit has first and second output terminals. In other words, the claimed decoder circuit outputs at least two different control outputs, while Suzu's circuit can output only one control output.

The rejection of claim 1 under 35 USC 102(b) on Suzu should be withdrawn because Suzu does not teach or suggest the claimed first and second output terminals.

The remaining rejection relies on Suzu and thus should be withdrawn as well because Suzu does not provide the teachings for which it is cited.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **247322002200**.

Respectfully submitted,

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